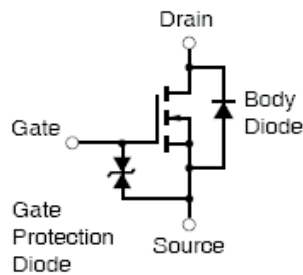
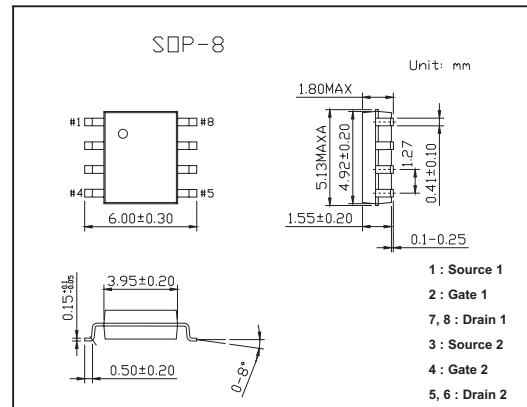


## MOS Field Effect Transistor

### KPA1764

#### ■ Features

- Dual chip type
- Low on-state resistance  
 $R_{DS(on)1} = 27 \text{ m}\Omega$  TYP. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 3.5 \text{ A}$ )  
 $R_{DS(on)2} = 32 \text{ m}\Omega$  TYP. ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 3.5 \text{ A}$ )  
 $R_{DS(on)3} = 34 \text{ m}\Omega$  TYP. ( $V_{GS} = 4.0 \text{ V}$ ,  $I_D = 3.5 \text{ A}$ )
- Low input capacitance
- $C_{iss} = 1300 \text{ pF}$  TYP.
- Built-in G-S protection diode
- Small and surface mount package



#### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	60	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 7$	A
Drain Current (Pulse) *1	$I_D(\text{pulse})$	$\pm 28$	A
Total Power Dissipation (1 unit) *2	$P_T$	1.7	W
Total Power Dissipation (2 unit) *2	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current *3	$I_{AS}$	7	A
Single Avalanche Energy *3	$E_{AS}$	98	mJ

\*1  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

\*2 Mounted on ceramic substrate of  $2000 \text{ mm}^2 \times 1.1 \text{ mm}$

\*3 Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 30 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

## KPA1764

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0			10	μ A
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μ A
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A	5.0	9		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A		27	35	m Ω
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3.5 A		32	42	m Ω
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 3.5 A		34	46	m Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1 MHz		1300		pF
Output Capacitance	C <sub>oss</sub>			230		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			110		pF
Turn-on Delay Time	t <sub>d(on)</sub>			15		ns
Rise Time	t <sub>r</sub>	I <sub>D</sub> = 3.5 A, V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 30 V, R <sub>G</sub> = 10 Ω		69		ns
Turn-off Delay Time	t <sub>d(off)</sub>			65		ns
Fall Time	t <sub>f</sub>			27		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 7.0A, V <sub>DD</sub> = 48V, V <sub>GS</sub> = 10 V		29		nC
Gate to Source Charge	Q <sub>GS</sub>			3.6		nC
Gate to Drain Charge	Q <sub>GD</sub>			7.4		nC
Body Diode forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 7.0 A, V <sub>GS</sub> = 0		0.84		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 7.0 A, V <sub>GS</sub> = 0 V		40		ns
Reverse Recovery Charge	Q <sub>rr</sub>		di/dt = 100 A/ μ s		66	